REMARKS

Claims 1 and 6 stand rejected under 35 U.S.C. §102(b) as being anticipated by or, in the alternative under 35 U.S.C. 103(a) as obvious over, Thaik (U.S. Pat. No.: 5,285,116). Specifically, regarding the rejection of claims 1 and 6 under 35 U.S.C. §102(b), the Examiner stated:

> Under 35 U.S.C. 102(b), Thaik in Figs. 4 – 7 discloses a pre-driver (24 and 26 in Fig. 4) providing an unbalanced output drive capability, comprising: a first data path (24 in Fig. 4) having a plurality of transistor output stages (including columns of transistors in Fig. 5A); a second data path (26 in Fig. 4) having a plurality of output stages (including columns of transistors in Fig. 6B); and a plurality of switches (where a "switch" is distinguished from a "transistor" and broadly interpreted as a unit that may include multiple transistors that are commonly controlled by a signal, such as N2 or N3 in Figs. 5A and 6B), each switch for (for example, a switch comprising 51 and 102 commonly controlled by N2, similar to a double-pole, single-throw switch unit) for controlling (via, for example, N2) the conductivity of a pair (for example, the lower second columns of Figs. 5A and 6A) of the plurality of output stages in response to the level of conductivity of a subsequent driver output stage (or to signals indicative of the strength of the output transistors in an output device) (for example, N2 is derived from an output buffer 20; see column 16, lines 4-6), wherein one of said pair of output stages is connected to said first data path (for example, the lower second column of Fig. 5A within 24) and another of said pair of output stages is connected to said second data path (for example, the lower second column of Fig. 6B within 26).

Regarding the rejection of claims 1 and 6 under 35 U.S.C. §103(a), the Examiner stated:

> In the alternative, under 35 U.S.C. 103(a), if the "switch" above is interpreted as a switching "transistor" (with reference to 114 or 116 in Fig. 7 of the instant application), Thaik fails to disclose the limitation "each switch" as recited in claims 1 and 6; however, the Thaik's combination of 51 in Fig. 5A and 102 in Fig. 6B, both controlled by N2, would be an obvious variant of "each switch" as recited in claims 1 and 6, since both variants control the conductivity of a pair of output states in different data paths simultaneously via a common control signal.

Furthermore, in discussing Applicants previous arguments, the Examiner stated:

> In response, it is noted that the predriver units 24 and 26 in Fig. 4 of Thaik, per se, clearly represent two structurally distinct data paths within the buffer 20. The unit 26 provides a path for the DRV-HIGH signal, which is related to the DATA SIGNAL; the unit 24 provides a path for the DRV-LOW-B signal, which is also related to the DATA SIGNAL. See for example, Thaik, column 5, lines 15 – 19. Therefore, Thaik anticipates the first and second data paths, as recited in claims 1 and 6. Similar response is presented for the Applicants' arguments regarding claims 2 – 5 and 7 – 9.

Claims 1 and 6 are each amended to recite that the first data path carries a data signal and that the second data path carries a delayed version of the data signal. Support for the instant amendment can be found at paragraph [0045] of the specification. It is respectfully submitted that Thaik fails to teach, disclose, or suggest first and second data paths which carry a data signal and a delayed version of the data signal, respectively.

In contrast, Thaik discloses an output buffer 20 that receives an input signal (i.e., DATA SIGNAL) and produces an output signal (i.e., DATA0) responsive to the input signal. The output buffer 20 includes a tri-state control stage 22, which depending on the input signal's state transition, provides a drv-low-B signal to a pull-up pre-driver 24 or a drv-high signal to a pull-down pre-driver 26 (column 5, lines 16 – 19).

If the output signal transitions from a "1" to a "0", pre-driver 24 turns on at least one of transistors 28, 30, and/or 32 (column 5, lines 19 – 22). More specifically for a transition from "1" to "0", the drv-low-B signal goes low and signal DN1 always goes high (column 7, lines 7 – 9), thus activating transistor 28 and pulling the output signal DATA0 to Vss. Signals DN2 and DN3 may also go high, depending upon the state of signals P2 and P3 (column 7, lines 60 – 64 and column 8, lines 39 – 43).

If the output signal transitions from a "0" to a "1", a pull-down pre-driver 26 turns on at least one of transistors 34 and/or 36 (column 5, lines 29 – 31). More specifically for a transition from "0" to "1", the drv-high signal goes high and the signal UP1B always goes low (column 10, lines 11 – 14), thus activating transistor 34 and pulling the output signal DATA0 to Vcc. Signal UP2B may also go low, depending upon the state of signal N2 and N3 (column 10, line 64 to column 11, line 1).

It is respectfully submitted that Thaik fails to teach or suggest that either the drv-low-B signal is a delayed version of the drv-high signal, or that the drv-high signal is a delayed version of the drv-low-B signal. In contrast, Thaik teaches that the function of input buffer 20 is to drive the output signal within an acceptable switching delay time and noise margin (column 5, lines 5 – 9). To accomplish this function, the various transistors (e.g., 28, 30, 32, 34, 36) are controlled so that the output signal is either being pulled up or being pulled down, but not both. (See, for example, column 5, lines 39 – 50). When the output buffer 20 transitions from a logic "1" to a logic "0", transistors 28, 30, and/or 32 are activated (i.e., drv-low-B is low) and transistors 34 and 36 are deactivated (i.e., drv-high is high). (See column 5, lines 18 – 21.) When the output buffer 20 transitions from a logic "0" to a logic "1", transistors 34 and/or 36 are activated (i.e., drv-high

is low) and transistors 28, 30, and 32 are deactivated (i.e., drv-low-B is high). (See column 5, lines 29 – 31.) If both the drv-low-B and drv-high signals were low, transistors 34 and 28, for example, would be activated at the same time and a short circuit condition would exist.

For the reasons discussed above, Thaik fails to teach, disclose, or suggest first and second data paths which carry a data signal and a delayed version of the data signal, respectively. Thus, it is believed that claims 1 and 6 are in condition for allowance. Accordingly, it is respectfully requested that the rejection of claims 1 and 6 pursuant to 35 U.S.C. 102(a) and 35 U.S.C. 103(b) in view of Thaik be withdrawn.

Claims 2 – 5 stand rejected under 35 U.S.C. §102(b) as being anticipated by Thaik (U.S. Pat. No.: 5,285,116). More specifically, the Examiner stated:

> Thaik in Figs. 4 – 7 discloses a method of providing an unbalanced output drive capability to correct for output skews in subsequent amplification stages, comprising: providing a plurality of output drive/pre-driver stages (for example, columns of transistors in Fig. 5A and 6B) on a first data path and on a second data path (24 and 26 in Fig. 4, respectively); generating a two-bit code/signal (for example, N2 and N3) representative of the relative strength of the n-channel and p-channel transistor in an output device (including 28, 30, 32, 34, and 36 in Fig. 4; see also column 16, lines 4 – 6 which discloses that the signals N2 and N3 are derived from an output buffer 20 in Fig. 4, which includes the output device); controlling in pairs, or enabling, the number of output drive/pre-driver stages on said first and second data paths that are activated (for example, N2 and N3 activate in pairs the output stages in Figs. 5A and 6B) in response to the amount of skew represented by the two-bit code/signal (see, for example, column 5, lines 62-64), wherein at least a first pair (for example, the lower first columns of Figs. 5A and 6B) of said output stages is controlled by the first bit (for example, N3) of said two-bit signal and at least a second pair (for example, the lower second columns of Figs. 5A and 6B) of said output stages is controlled by the second bit (for example, N2 of said two-bit signal), and wherein one output stage of said pairs is connected to said first data path (for example, the lower second column of Fig. 5A in 24) and another of each of said pairs of output stages is connected to said second data path (for example, the second column of Fig. 6B in 26), wherein said pre-driver produces an unbalanced output from the pre-driver (for example, the output DN1 in Fig. 5A; column 6, lines 36 – 38); and inputting a data signal to the output device through the pre-driver (in Fig. 4, DATA SIGNAL is inputted to the output device through 24 and 26, which include Figs. 5A and 6B).

Claims 2, 4, and 5 are each amended to recite that the first data path carries a data signal and that the second data path carries a delayed version of the data signal. As discussed above, Thaik fails to teach, disclose, or suggest a first data path carrying a data signal and a second data path carrying a delayed version of the data signal. Thus, it is believed that claims 2, 4, and5 are

in condition for allowance. Claim 3 depends from allowable claim 2, and thus, is also believed to be in condition for allowance. Accordingly, it is respectfully requested that the rejection of claims 2 – 5 pursuant to 35 U.S.C. 102(a) in view of Thaik be withdrawn.

Claims 7 – 9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ong (U.S. Patent Number 5,798,970) in view of Thaik (U.S. Pat. No.: 5,285,116). However, as recognized by the Examiner, Ong does not supply the teachings missing from Thaik in terms of the pre-driver:

> Ong does not disclose a pre-driver providing an unbalanced output drive capability, comprising: a first pre-driver data path having a plurality of output transistors; a second pre-driver data path having a plurality of output transistors; and a plurality of switches, each switch for controlling the conductivity of a pair of said plurality of output transistors in response to signals indicative of the strength of output transistors in the output driver, wherein one of said pair of output transistors is connected to said first pre-driver data path and another of said pair of output transistors is connected to said second pre-driver data path, said pre-driver providing said data signal to said output driver.
>
> Thaik discloses a pre-driver as in claims 1 and 6 above. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the computer system on Ong by incorporating the pre-driver of Thaik, for the purpose of controlling the switching speed with maximum efficiency across process, temperature and supply voltage variations (Thaik, column 1, lines 6 – 13).

Claims 7 – 9 are each amended to recite that the first data path carries a data signal and that the second data path carries a delayed version of the data signal. As discussed above, Thaik fails to teach, disclose, or suggest a pre-driver having a first data path carrying a data signal and a second data path carrying a delayed version of the data signal. As noted by the Office, Ong fails to disclose the missing teachings. Thus, it is believed that claims 7 – 9 are in condition for allowance and it is respectfully requested that the rejection of claims 7 – 9 pursuant to 35 U.S.C. §103(a) over Ong in view of Thaik be withdrawn.

Applicants have made a diligent effort to place the instant application in condition for allowance. Accordingly, a Notice of Allowance for claims 1 – 9 is earnestly requested. If the Examiner is of the opinion that the instant application is in condition for disposition other than by allowance, he is respectfully requested to contact applicants' attorney at the phone number listed below so that additional changes to the claims may be discussed.

Respectfully submitted,

Richard J. Coldren

Richard J. Coldren
Reg. No. 44,084
Thorp Reed & Armstrong LLP
One Oxford Centre
301 Grant Street, 14th Floor
Pittsburgh, PA 15219-1425
(412) 394-2442

Dated: 7 April 2005

Attorneys for Applicant